WHAT IS CLAIMED IS:

1. A semiconductor device comprising, in combination, a silicon substrate having a first and second surface; a first epitaxially deposited layer formed atop said first surface and having impurities of the n or p conductivity type uniformly distributed throughout the volume of said first layer; a second epitaxially deposited layer deposited atop the surface of said first layer and having impurities of the same type as those in said first layer uniformly distributed therethrough; the concentration of impurities in said second layer being greater than the concentration of impurities in said first layer; and a plurality of diffusions of a conductivity type opposite to that of said second layer uniformly distributed into the surface of said second layer and defining p-n junctions therein.

2. The device of claim 1 wherein the resistivity of said second layer is higher than that of said first layer.

3. The device of claim 1 wherein the thickness of said first layer is more than that of said second layer.

4. The device of claim 2 wherein the thickness of said first layer is more than that of said second layer.

5. The device of claim 1 wherein the total thickness of said first and second layers is less than the thickness of a single epitaxial layer designed to block the same voltage.

6. The device of claim 2 wherein the total thickness of said first and second layers is less than the thickness of a single epitaxial layer designed to block the same voltage.

7. The device of claim 3 wherein the total thickness of said first and second layers is less than the thickness of a single epitaxial layer designed to block the same voltage.

8. The device of claim 4 wherein the total thickness of said first and second layers is less than the thickness of a single epitaxial layer designed to block the same voltage.

9. The device of claim 8 wherein said device is a vertical conduction power MOSFET.

10. A vertical conduction power MOSFET device having a reduced on-resistance; said device comprising a silicon substrate having a drain electrode on the bottom surface thereof, and an epitaxially deposited layer on the upper surface of said substrate; said epitaxial deposited layer having a graded concentration of one of the conductivity types from its top free surface to its bottom; an upper portion of said epitaxial layer extending from its free surface receiving a P-N junction which at least partly defines said power MOSFET and having an average impurity concentration which is more than the average concentration of the bottom portion of said epitaxial layer; said bottom portion of said epitaxial layer comprising more than 50% of the total thickness of said epitaxial layer.

11. The device of claim 10 wherein said lower and upper portions of said epitaxial layer comprise respective separately deposited first and second layers of respective uniform concentration or the upper portion of uniform doped epitaxial layer receives extra same type ion implantation and drive process.

12. The device of claim 11 wherein the total thickness of said first and second layers is less than the thickness of a single epitaxial layer designed to block the same voltage.